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An Ultra-compact D-Band SiGe Low Noise Amplifier for Array Integration

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***Abstract*—We present a compact four-stage, 123 to 164 GHz low-noise amplifier (LNA) fabricated in a 90-nm SiGe BiCMOS technology. The LNA uses common-emitter and common-base stages with staggered tuning to achieve high gain and wide bandwidth across D-band while minimizing area consumption. The LNA demonstrates a maximum gain of 19.7 dB with a minimum noise figure of 7.0 dB while consuming 37.6 mW and 0.015 mm^2 of area. To our knowledge, this work has the lowest active area consumption for reported LNAs in D-band while demonstrating comparable performance and power consumption to earlier literature, making it suitable for highly scaled receiver arrays.**

***Index Terms*—D-band, millimeter wave, low-noise amplifier (LNA), silicon germanium (SiGe), BiCMOS, HBT**

I. Introduction

Wireless systems will increasingly unify sensing and communication through common apertures requiring radio architectures that adapt to the requirements of different tasks while cooperatively taking advantage of the wide spectrum availability in the frequency bands from 30 GHz (mm-wave) up to 300 GHz (THz) [1]. Cooperation enhances communication through spatial localization and improves radar by distributed coordination in a dynamic channel environments with a MIMO system. However, the power consumption of transmit and receive arrays increases at higher frequency and would be prohibitive in applications such as handsets where the power budget is limited [2]. The receiver blocks that dominate power consumption in higher frequency bands are typically low-noise amplifiers (LNA) and the LO multiplier chain.

In this work, a SiGe HBT LNA fabricated in a 90-nm SiGe BiCMOS technology is presented to cover 110-170 GHz. Due to the array element spacing demanded at 170 GHz, e.g. 0.8 mm, it has a compact form suitable for integration in digital beamforming front-ends as illustrated in Fig. 1a and Fig. 1b. Because of low conversion gain of passive mixers, the noise figure seen at the input of the mixer can be greater than 15 dB. The design focuses on maximizing gain per area and noise figure through noise measure matching. By reducing the number of stages, both the size and overall power consumption is also reduced.

II. Design

The circuit is illustrated in Fig 2 and indicates a 4-stage LNA composed of a common-emitter first stage, a common-base second stage, followed by two identical common-emitter stages. All stages are designed with 50 Ω input and output impedances. The first stage is used to provide noise performance and wide-band input matching, while the other stages are used to shape the gain and increase output power with their contributions to gain shown in Fig. 4.

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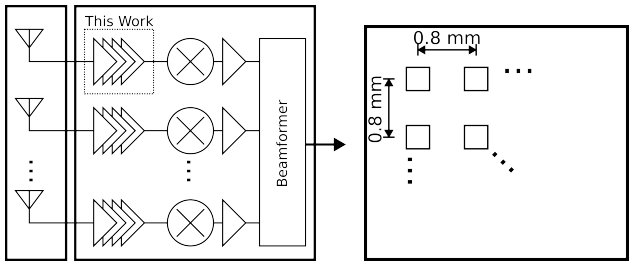

Fig. 1: (a) Diagram of monolithic integration between the LNA of this work and a SiGe BiCMOS receiver system with external antenna packaging, and (b) receiver system in 2-dimensional tiling with half-wavelength spacing requirements.

A. First Stage Design

The first stage uses a transistor with an emitter length of 2 um in CBEBC configuration. The length of the transistor emitter was chosen to facilitate high-bandwidth input matching with the intention of providing a predictable interface with an antenna for integration. The transistor's base impedance is 42.8 - j59.6 Ω at 140 GHz, which is easily matched to 50 Ω with a short series line for low loss and matching bandwidth instead of a large transformer.

The chosen bias provides the highest available gain in anticipation of loss from the implementation of the matching network. The bias also allows the use of fewer stages to achieve sufficient gain to suppress the noise contributions from the following integrated subsystems, such as a mixer, minimizing area consumption. To evaluate this trade-off, the cascaded noise figure is used, since it is related to the noise measure, M, which is invariant to transistor embedding [3], related in the following equation.

$$F_\infty = F + \sum_{k\geq 1}^{\infty} \frac{(F-1)}{G_A^k} = \frac{F-1}{1-1/G_A} + 1 = M + 1. \quad (1)$$

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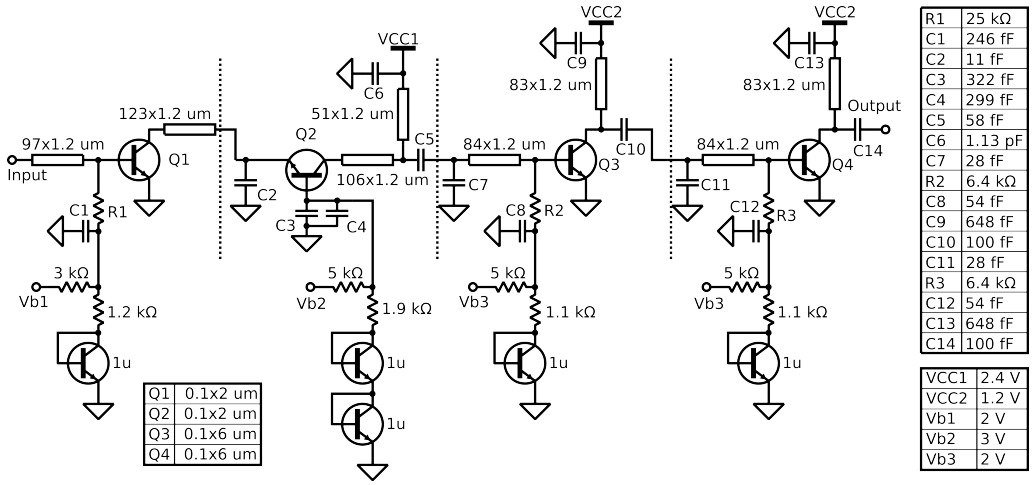


Fig. 2: Schematic of proposed low-noise amplifier with biasing circuity.

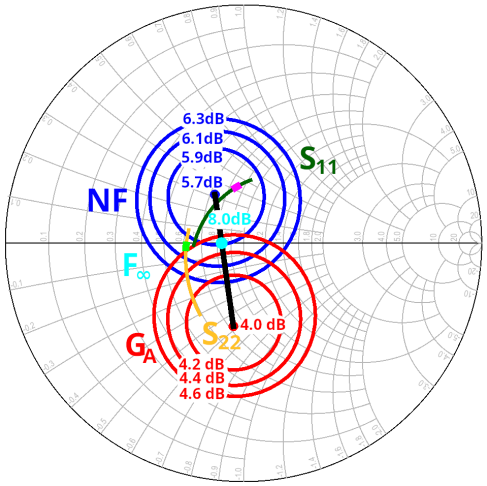


Fig. 3: Minimum noise measure impedance match with first LNA stage at 158 GHz. Input and output impedances are shown from 110-170 GHz with 158 GHz marked.

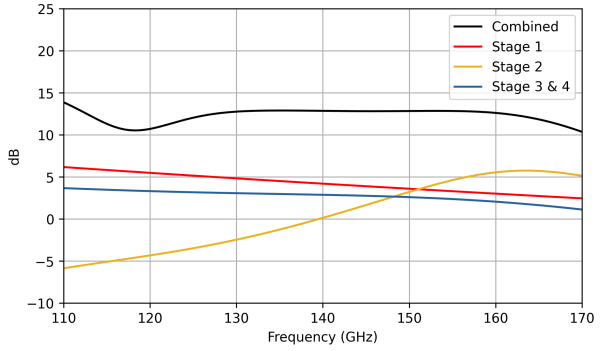


Fig. 4: Simulated gain per stage contributions with staggered tuning and combined gain of full 4-stage LNA.

The minimum cascaded noise figure ($F_{\infty,min}$) at the chosen collector current at 4.0 mA is 7.1 dB with 5.7 dB of available gain, while the minimum noise measure at the optimum bias of 0.9 mA is 5.7 dB with 4.4 dB of gain at 170 GHz. The chosen bias yields an implemented stage gain at 170 GHz of 2.4 dB, which gives a reasonable margin for the fabrication and simulation deviation. The stage's cascaded noise figure is 9.2 dB at 170 GHz.

The first stage implements staggered tuning where the input match is tuned for a slightly lower frequency than the output, which is intended to work with the second stage, which supplements gain at high frequencies. This match is illustrated in Fig. 3, along with the minimum noise measure impedance match. Since the minimum noise figure and the available gain decrease at high frequencies, the optimum noise measure impedance was matched at a higher frequency to extract the transistor noise measure performance.

B. Second Stage Design

The second stage is a 2-um emitter HBT in common-base configuration (CBEBC) for increased gain at the high-frequency edge of the band to achieve gain flatness in the D-band. A matched common-base configuration was chosen over a direct connection to the first stage as a cascode, since it provides higher gain for the power consumed, avoiding the need to add additional stages to meet the gain requirement of the larger system. Bias current supplied through the common-base stage is reused by the first common-emitter stage. This DC connection obviates need for a blocking capacitor, which reduces area consumption. This transistor has the same collector current as the first stage.

C. Third and Fourth Stage Design

The identical third and fourth stages use 6 um emitter CBEBC transistors in common-emitter configuration to increase the maximum output power and to increase gain with the remaining available area. The transistor size was chosen to obtain an output 1-dB compression point of about 0 dBm, and each has 9.4 mA of collector current.

D. Circuit Implementation

Due to the need to minimize the area of the LNA, techniques to improve performance with large passives were avoided. For example, inductive degeneration can simultaneously match both noise and gain, but it was not used due to the high loss and area trade-off. Although techniques such as coupled lines yield high bandwidth with similar performance to transmission lines [4], simple transmission line matching in an LNA with staggered tuning, transistor sizing, and bias tuning can achieve similar results with shorter and thinner lines to minimize area.

For the presented LNA test structure, a 50 Ω transmission line of 450 μm length connects the LNA to the output pad, as shown in Fig. 5. Due to the small size of the LNA, the line gives physical clearance for probing. In D-band, it has a measured insertion loss ranging from 0.5 dB to 1.7 dB, while return loss remains under 14.6 dB.

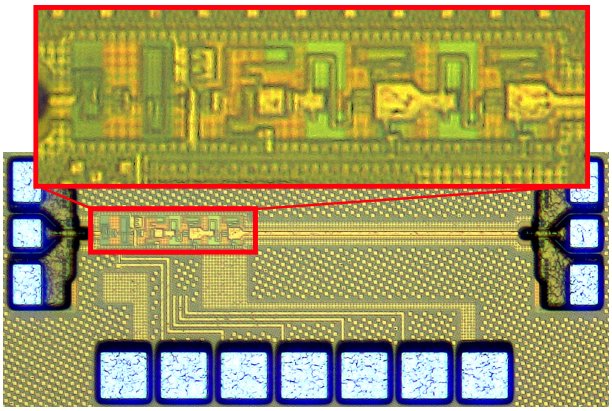


Fig. 5: Micrograph of LNA test structure with output extension and chip dimensions of 395 um x 975 um and magnification of integrable LNA core with size of 60 um x 245 um.

III. Measurement Results

Measurements were made on the LNA, with voltage biases shown in Fig. 2. The LNA itself consumed 35.7 mW, while the biasing circuits consumed 1.9 mW, leading to 37.6 mW of total power consumption. Because the LNA was intended to integrated into a larger system with voltage supply, the biases were set by voltage through biasing circuits. The simulated total collector current is 22.8 mA, while the measured collector current is 25.5 mA. For all measurements and simulations, the output extension line was not de-embedded from the results.

A. S-Parameter Measurements

S-parameters were measured from 110 GHz to 170 GHz on a Keysight N5277A network analyzer with D-band (110-170 GHz) VDI frequency extenders and WR-06 probes. The LNA achieves more than 12 dB of gain across D-band, with a maximum of 19.7 dB at 118 GHz. The gain remains in a 3-dB range from 123 to 164 GHz. In addition to higher gain, there is also a downward frequency shift of approximately 15%.

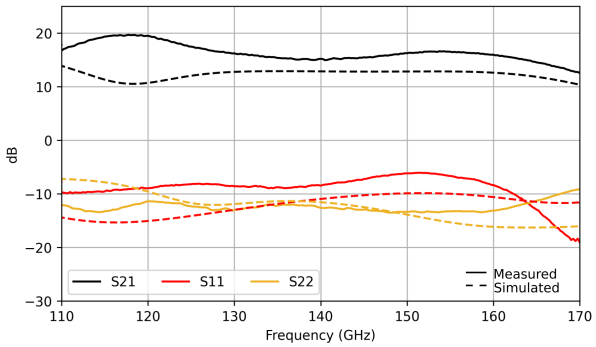


Fig. 6: S-parameter Measurement.

B. Power Measurement

Power measurements in D-band were made on the LNA by down-converting continuous wave output from the LNA to a VDI WR6.5SAX-M spectrum analyzer extender and detecting narrow-band power with a Keysight N9030B spectrum analyzer. The input to the LNA was generated with the network analyzer as the signal source, up-converted with the D-Band frequency extenders, and then attenuated with a Mi-Wave 511D programmable rotary vane attenuator followed by an isolator. For sweeping across input powers, the programmable attenuator was used to control power due to extreme sensitivity to input power changes on the extenders. The generated input power level over frequency was calibrated using a VDI PM5B power meter as the reference. Then, the down-conversion gain to the spectrum analyzer was calibrated using the known power from the calibrated input chain.

The power measurements across frequency shown in Fig. 7a are in agreement with the gain from S-parameter measurement for small input power levels. The measurement is presented as 1-dB compression points of the LNA in Fig. 7b, which are close to simulation. The lower input compression and higher output compression than simulation are consistent with the higher observed gain. The 1-dB input compression points range from -18.4 dBm to -11.7 dBm.

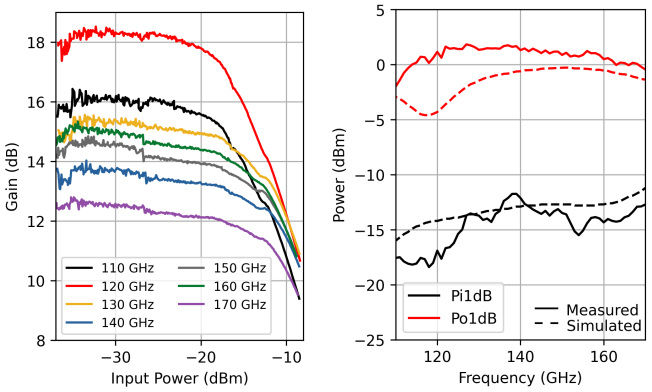
TABLE I: Comparison with D-band Silicon LNAs

Reference	**This Work**	[4]	[5]	[6]	[7]	[8]
Technology	90-nm SiGe	90-nm SiGe	90-nm SiGe	55-nm SiGe	130-nm SiGe	130-nm SiGe
Freq. (GHz)	144	139.8	140	140	140	140
BW_{3dB} (GHz)	41	37.6	28	70	52	23.2
Max. Gain (dB)	19.7	26.5	30	23	32.6	32.8
P_{i1dB} (dBm)	-13.4	-31	-	-21.3	-37.6	-28.6
NF (dB)	7.0-9.3	7.2	6.2	5-6.5	4.8-6.1	7.8*
P_{DC} (mW)	37.6	20.6	45	60	28	39.6
Core Area (mm^2)	0.015	0.69 †	0.11	0.109	0.6	0.075†

* Simulated † Die Area

C. Noise Measurement

Noise measurements in D-band were made using an Eravant STZ-06-IT2 WR-06 hot-cold noise source, with a nominal



(a) (b)

Fig. 7: (a) Measured gain across input power with frequencies, and (b) Measured LNA output and input 1-dB compression powers.

ENR of 15 dB, through the Y-factor technique. The down-conversion equipment and calibrated reference planes are shown in Fig. 8. The dual side-band detection was done at a 1 GHz IF with a 240 kHz RBW. The noise contribution of the probe losses was removed by calculation, since the noise calibration reference plane was set at the input of the down-conversion chain. The probe loss was obtained with a measurement in a back-to-back configuration with a pair on an on-chip through.

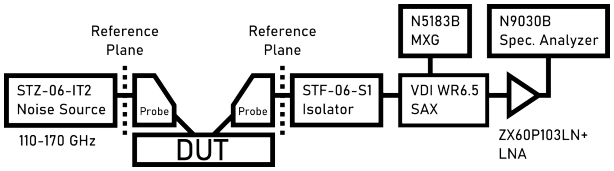


Fig. 8: LNA Measurement Setup.

As shown in Fig. 9, the measured noise figure remains below 9.3 dB for the entire D-band, while the lowest observed noise figure was 7.0 dB at 145 GHz. The noise is lower than simulated and a source of error may come from scalar de-embedding of the probe gain and noise contribution, since their losses were obtained with a scalar power measurement. Monte Carlo analysis on process and mismatch variation show that transistor does not totally account for the difference, with a 1.1 dB standard deviation for gain and a 0.4 dB standard deviation for noise figure. Bias sweeps in both simulation and measurement did not replicate the difference. The estimated noise measurement uncertainty is ± 0.7 dB over 2σ at 140 GHz. A reason that would explain both higher gain and lower noise than in simulation is that the simulation overestimates the loss of matching networks. The LNA was simulated with EMX in parts by stage, which could be a source of this difference.

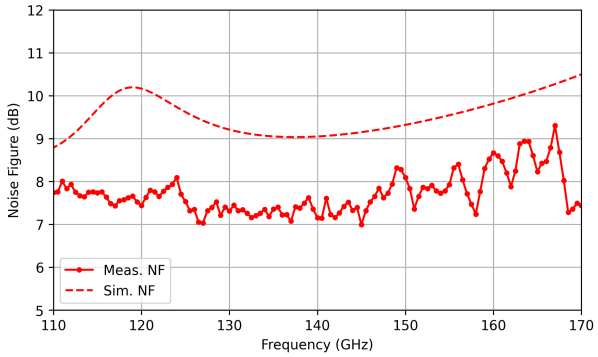


Fig. 9: Measured Noise Figure.

IV. Conclusion

A 4-stage D-band LNA is presented. Gain greater than 12 dB across D-band is achieved by designing multiple cascaded stages with staggered tuning to provide gain at multiple bands. A minimum noise figure of 7.0 dB is demonstrated along with a 1-dB input compression power of -13.4 dBm. The LNA achieves this performance with an extremely low area consumption of only 0.015 mm^2, making it suitable for highly scaled receiver systems.

Acknowledgment

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